Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Canceled)
2. (Previously Canceled)
3. (Previously Canceled)
4. (Previously Canceled)
5. (Previously Canceled)
6. (Previously Canceled)
7. (Previously Canceled)
8. (Previously Canceled)
9. (Previously Canceled)
10. (Previously Canceled)
11. (Previously Canceled)
12. (Previously Canceled)
13. (Previously Canceled)
14. (Previously Canceled)
15. (Previously Canceled)
16. (Previously Canceled)
17. (Previously Canceled)
18. (Previously Canceled)
19. (Previously Canceled)

20. (New) A memory access system comprising:

a register holding at least two packed objects for use in identifying respective memory addresses;

address generating circuitry for generating at least first and second memory addresses from said at least two packed objects;

a first memory access unit that accesses a memory using said first and second addresses; and

a second memory access unit operable to access said memory;

wherein when said second memory access unit is inactive, said second address is issued to said second memory access unit to allow simultaneous memory accesses to be made by the first and second memory access units.

21. (New) The memory access system according to claim 20, wherein the second memory address is not related to the first memory address.

22. (New) The memory access system according to claim 20, wherein the register is an index register and wherein said at least two packed objects are offset objects for combining with a base value held in a second register to generate said first and second addresses.

23. (New) The memory access system according to claim 22, wherein the base value comprises two packed objects representing two base addresses which are combined respectively with the packed offset objects in the index register to generate said first and second addresses.

24. (New) The memory access system according to claim 22, wherein the address generating circuitry comprises first and second addition circuits for respectively adding the

packed objects in the first register with the contents of the second register to generate said first and second addresses.

25. (New) The memory access system according to claim 20, wherein said at least two packed objects represent respective base addresses, which identify respective memory addresses when combined with an offset in a second register.

26. (New) The memory access system according to claim 20, wherein the register holds four offset objects, two of which are selected by the address generating circuitry for generating said first and second addresses.

27. (New) The memory access system according to claim 20, wherein the register holds four offset objects for use in respectively identifying four memory addresses.

28. (New) The memory access system according to claim 20, wherein the register holds eight offset objects, a number of which are selected for use in generating a corresponding number of memory addresses.

29. (New) The memory access system according to claim 20, further comprising:

a second register, the first and second registers having the same predetermined bit capacity and being capable of holding one or more objects depending on the bit length of the object.

30. (New) A method of generating addresses for accessing a data memory, comprising:

receiving a base value representing a base address;

receiving an index value;

wherein at least one of the base value and the index value include at least two packed objects;

combining the base value and the index value to generate first and second addresses;

providing the first address to a first memory access unit that accesses a memory using said first address; and

providing the second address to a second memory access unit when said second memory access unit is inactive,

wherein said first and second memory access units simultaneously access said memory using said first and second addresses.

31. (New) The method according to claim 30, wherein the second memory address is not related to the first memory address.

32. (New) The method according to claim 30, further comprising identifying locations of the base value and the index value from a single computer instruction.

33. (New) The method according to claim 30, wherein the said at least two packed objects are offset objects for combining with the base value.

34. (New) The method according to claim 33, wherein the base value comprises two packed objects representing two base addresses which are combined respectively with the offset objects to generate said first and second addresses.

35. (New) The method according to claim 30, wherein said at least two packed objects represent respective base addresses, which identify respective memory addresses when combined with an the index value.